1. An apparatus for monitoring the latency of a component that generates a ready signal after completing an assigned task, the apparatus comprising:

control logic adapted to interface with the component; and

a response time measurement circuit connected to the control logic and the component, the response time measurement circuit being adapted to provide a measured response time to the control logic.

2. The apparatus of claim 1, wherein the response time measurement circuit comprises a phase detector.

3. The apparatus of claim 2, wherein the phase detector comprises a plurality of transparent latches each having a data input, a data output, and a clock input, the data input of each transparent latch being connected to receive a ready signal of a component whose response time is being measured and the clock input of each transparent latch being connected to receive a respective clock signal generated at a different point of a response window such that the data outputs of the transparent latches indicate the respective portion of the response window in which a data ready signal is received.

4. The apparatus of claim 3, wherein the transparent latches are data flip-flops.

5. The apparatus of claim 3, further comprising a logic circuit connected to the data output of at least one of the transparent latches such that the logic circuit generates an excessive latency drift signal when the data

output indicates that the data ready signal has drifted in excess of a predetermined threshold.

6. A component controller comprising:

control logic adapted to interface with the component;

a response time measurement circuit connected to the control logic and the component for detecting an excessive latency drift of the component in responding to a command and providing an excessive latency drift signal to the control logic; and

a local memory connected to the control logic;

wherein the control logic is adapted to store information on the component in the local memory when an excessive latency drift signal is received.

7. The controller of claim 6, wherein the component has a programmable response time.

8. The controller of claim 6, wherein the component is a memory circuit.

9. The controller of claim 8, wherein the memory circuit is a programmable response time memory circuit.

10. The controller of claim 9, wherein the programmable response time memory circuit is an SLDRAM memory circuit.

11. The controller of claim 10, wherein the control logic is adapted to recalibrate at least one SLDRAM memory circuit upon receipt of an excessive latency drift signal from an SLDRAM memory circuit.

12. The controller of claim 6, wherein the component information comprises an identification code of the component and the time at which the excessive latency drift signal is provided to the control logic.

13. A memory controller comprising:

control logic adapted to interface with a memory component and to generate a response window signal when the memory component is commanded to retrieve data therein;

an offset clock generator connected to receive the response window signal for generating a plurality of phase clock signals;

a phase detector comprising a plurality of transparent latches each having a data input, a data output, and a clock input, the clock input of each transparent latch being connected to receive a respective phase clock signal from the offset clock generator, and the data input of each transparent latch being connected to receive a data ready signal from the memory component, the data ready signal being provided by said memory component when the data is available;

a logic circuit having an input connected to an output of the transparent latches and an output connected to the control logic for generating an excess latency drift signal; and

a local memory connected to the control logic for storing component information for a memory component which caused the excess latency drift signal to be generated.

14. The controller of claim 13, wherein the memory component is an SLDRAM and the control logic is adapted to recalibrate at least one SLDRAM memory component upon receipt of an excess latency drift signal.

15. The controller of claim 14, wherein the phase clock signals are evenly distributed over a response window initiated by said response window signal.

16. The controller of claim 15, wherein the phase clock signals are distributed over an entire response window initiated by said response window signal.

17. The controller of claim 16, wherein the response window consists of one memory clock cycle.

18. A computer system comprising:

a processor;

a memory component; and

a memory control system connected to and operative with the processor and the memory component, the memory control system comprising:

control logic adapted to communicate with the memory component;

a response time measurement circuit connected to the control logic and the component for detecting an excessive latency drift of the component in responding to a command and providing an excessive latency drift signal to the control logic; and

a local memory connected to the control logic;

wherein the control logic is adapted to store information on the component in the local memory when an excessive latency drift signal is received.

19. The controller of claim 18, wherein the component is a memory circuit.

20. The controller of claim 19, wherein the memory circuit is an SLDRAM memory circuit.

21. The controller of claim 20, wherein the control logic is adapted to recalibrate at least one SLDRAM memory circuit upon receipt of an excessive latency drift signal from an SLDRAM memory circuit.

22. The controller of claim 18, wherein the component information comprises an identification code of the component and the time at which the excessive latency drift signal is provided to the control logic.

23. A computer system comprising:

a processor;

a memory component; and

a memory control system connected to and operative with the processor and the memory component, the memory control system comprising:

control logic adapted to interface with a memory component and to provide a response window signal at the start of a response window;

an offset clock generator connected to receive the response window signal for generating a plurality of phase clock signals;

a phase detector comprising a plurality of transparent latches each having a data input, a data output, and a clock input, the clock input of each transparent latch being connected to receive a respective phase clock signal from the offset clock generator, and the data input of each transparent latch being connected to receive a data ready signal from the memory component;

a logic circuit having an input connected to a data output of at least one of the transparent latches and an output connected to the control logic for generating an excess latency drift signal; and

a local memory connected to the control logic;

wherein the control logic is adapted to store information pertaining to the component causing the excess latency drift signal to be generated.

24. The controller of claim 23, wherein the memory component is a programmable response time memory component and the control logic is adapted to recalibrate at least one programmable response time memory component upon receipt of an excess latency drift signal.

25. The controller of claim 24, wherein the phase clock signals are evenly distributed over a response window initiated by said response window signal.

26. The controller of claim 25, wherein the phase clock signals are distributed over an entire response window initiated by said response window signal.

27. The controller of claim 26, wherein the response window consists of one memory clock cycle.

28. A component controller comprising:

control logic adapted to interface with the component;

a response time measurement circuit connected to the control logic and the component for detecting an excessive latency drift and providing an excessive latency drift signal to the control logic; and

a local memory connected to the control logic;

wherein the control logic is adapted to store information on the component in the local memory when an excessive latency drift signal is received and to determine when the latency drift of component indicates that the component may need replacing or relocation.

29. The controller of claim 28, wherein the control logic determines that the component may need replacing or relocating by calculating short and long term averages of the time between excessive latency drifts and comparing the ratio of the averages to a predetermined threshold.

30. The controller of claim 28, wherein the control logic determines that the component may need replacing or relocating by calculating short and long term averages of the magnitude of the latency drifts and comparing the ratio of the averages to a predetermined threshold.

31. The controller of claim 28, wherein the control logic determines that the component may need replacing or relocating by calculating the standard deviation of the time between excessive latency drifts, counting a total number of latency drifts whose drift time is below a

first predetermined threshold based on the standard deviation; and comparing the total to a second predetermined threshold.

32. The controller of claim 28, wherein the control logic determines that the component may need replacing or relocating by calculating the standard deviation of the latency drift of the component, counting the total of the number of latency drifts that exceed a first predetermined threshold based on the standard deviation, and comparing the total to a second predetermined threshold.

33. A memory circuit controller comprising:

control logic adapted to interface with a plurality of memory circuits;

a response time measurement circuit connected to the control logic and the memory circuits for detecting an excessive latency drift and providing an excessive latency drift signal to the control logic;

a local memory connected to the control logic;

wherein the control logic is adapted to store failure information in the local memory when an excessive latency drift signal is received; and

wherein the control logic is further adapted to determine when the latency drift of one memory circuit indicates that the one memory circuit may need replacing or relocating by calculating the ratio of excessive latency drifts caused by the one memory circuit to the total number of latency drifts, and comparing the ratio to a predetermined threshold.

34. A computer system comprising:

a processor;

an output device connected to the processor;

a memory component; and

a memory control system connected to and operative with the processor and the memory component, the memory control system comprising:

control logic adapted to interface with the memory component;

a response time measurement circuit connected to the control logic and the component for detecting an excessive latency drift and providing an excessive latency drift signal to the control logic; and

a local memory connected to the control logic;

wherein the control logic is adapted to store information on the component in the local memory when an excessive latency drift signal is received, to determine when the latency drift of the component indicates that the component may need replacing or relocating and to send a message to the processor indicating which component may need replacing or relocating, and wherein the processor outputs the message to the output device.

35. The computer system of claim 34, wherein the control logic determines that the component may need replacing or relocating by calculating short and long term averages of the time between excessive latency drifts and comparing the ratio of the averages to a predetermined threshold.

36. The computer system of claim 34, wherein the control logic determines that the component may need replacing or relocating by calculating short and long term averages of

the magnitude of the latency drifts and comparing the ratio of the averages to a predetermined threshold.

37. The computer system of claim 34, wherein the control logic determines that the component may need replacing or relocating by calculating the standard deviation of the time between excessive latency drifts, counting a total number of latency drifts whose drift time is below a first predetermined threshold based on the standard deviation; and comparing the total to a second predetermined threshold.

38. The computer system of claim 34, wherein the control logic determines that the component may need replacing or relocating by calculating the standard deviation of the latency drift of the component, counting the total of the number of latency drifts that exceed a first predetermined threshold based on the standard deviation, and comparing the total to a second predetermined threshold.

39. A computer system comprising:

a processor;

an output device connected to the processor;

a plurality of memory components; and

a memory control system connected to and operative with the processor and the memory components, the memory control system comprising:

control logic adapted to interface with the memory components;

a response time measurement circuit connected to the control logic and the memory components for

detecting an excessive latency drift and providing an excessive latency drift signal to the control logic;

a local memory connected to the control logic;

wherein the control logic is adapted to store failure information in the local memory when an excessive latency drift signal is received; and

wherein the control logic is further adapted to determine when the latency drift of one component indicates that the one component may need replacing or relocating by calculating the ratio of excessive latency drifts caused by the one component to the total number of latency drifts, and comparing the ratio to a predetermined threshold.

40. A method for monitoring the latency drift of a component which generates a ready signal after completing an assigned task, comprising the steps of:

providing a plurality of transparent latches, each of the latches having a data input, a data output, and a clock input;

connecting the data input of each transparent latch to receive a ready signal of a component whose response time is being measured;

connecting the clock input of each transparent latch to receive a respective clock signal generated at a different point of a response window such that the data outputs of the transparent latches indicate the respective portion of the response window in which a data ready signal is received; and

detecting the respective data outputs of the transparent latches.

41. The method of claim 40, wherein the clock signals are distributed over the entire response window.

42. The method of claim 40, wherein the clock signals are evenly distributed.

43. The method of claim 40, wherein the response window consists of one clock cycle.

44. The method of claim 40, further comprising the step of connecting a logic circuit to the data output of at least one transparent latch to generate an excessive latency drift signal.

45. A method for monitoring the latency drift of a programmable response time memory component which generates a ready signal after completing a data retrieval operation, comprising the steps of:

providing a plurality of transparent latches, each of the latches having a data input, a data output, and a clock input;

connecting the data input of each transparent latch to receive a ready signal of a programmable response time memory component whose response time is being measured;

connecting the clock input of each transparent latch to receive a respective clock signal generated at a different point of a response window such that the data outputs of the transparent latches indicate the respective portion of the response window in which a data ready signal is received;

connecting a logic circuit to the data output of at least one transparent latch to generate an excessive latency drift signal;

observing the respective data outputs of the transparent latches to determine a latency drift when an excessive latency drift signal is received;

comparing the observed latency drift to a predetermined threshold; and

recalibrating at least one programmable response time memory component when the observed latency drift exceeds the predetermined threshold.

46. The method of claim 45, wherein the programmable response time memory component is an SLDRAM.

47. A method of determining when a component may need to be replaced comprising the steps of:

monitoring the latency drifts of a component;

storing component latency drift information;

comparing the stored latency drift information to a predetermined threshold; and

indicating the need for replacement when the stored latency drift information exceeds the threshold.

48. The method of claim 47, wherein the step of comparing the stored latency drift information to a predetermined threshold comprises:

calculating a short term average of the time between excessive latency drifts,

calculating a long term average the time between excessive latency drifts; and

comparing the ratio of the averages to a predetermined threshold.

49. The method of claim 47, wherein the step of comparing the stored latency drift information to a predetermined threshold comprises:

calculating a short term average of the magnitude of the latency drifts,

calculating a long term average of the magnitude of the latency drifts; and

comparing the ratio of the averages to a predetermined threshold.

50. The method of claim 47, wherein the step of comparing the stored latency drift information to a predetermined threshold comprises:

calculating the standard deviation of the time between excessive latency drifts;

counting a total of the number of latency drifts whose drift time is below a first predetermined threshold based on the standard deviation; and

comparing the total to a second predetermined threshold.

51. The method of claim 47, wherein the step of comparing the stored latency drift information to a predetermined threshold comprises:

calculating the standard deviation of the magnitude of the stored latency drifts;

counting a total of the number of latency drifts whose magnitude exceeds a first predetermined threshold based on the standard deviation; and

comparing the total to a second predetermined threshold.

52. A method of determining when a memory circuit in a system having a plurality of memory circuits may need to be replaced comprising the steps of:

monitoring the latency drifts of a memory circuit;

storing memory circuit latency drift information;

calculating the ratio of excessive latency drifts caused by one memory circuit to the total number of excessive latency drifts; and

comparing the ratio to a predetermined threshold.

53. A method for improving the reliability of a computer system comprising the steps of:

distributing a plurality of interchangeable components in a plurality of locations;

measuring the average time between excessive latency drifts for each component;

storing the average time;

repeating the distributing, measuring and storing steps at least once;

determining the global average time between excessive latency drifts for each component;

determining the global average time between excessive latency drifts for each location;

associating components with locations such that the components with the highest global average time between excessive latency drifts are assigned to respective locations with the lowest global average time between excessive latency drifts.

54. The method of claim 53 wherein the average time between excessive latency drifts for each component is measured in all locations.

55. The method of claim 53 wherein the average time between excessive latency drifts for each component is measured in two locations.

56. A method for improving the performance of a computer system having a plurality of interchangeable components and a plurality of component locations, the method comprising the steps of:

measuring the response time of each of the interchangeable components;

determining the frequency at which each of the component locations is accessed; and

associating components with component locations such that the components with the fastest response times are located in respective locations that are accessed the most frequently.

57. The method of claim 56, wherein the associating step is performed by physically placing components at component locations.

58. The method of claim 56, wherein the associating step is performed by logically placing components at component locations.